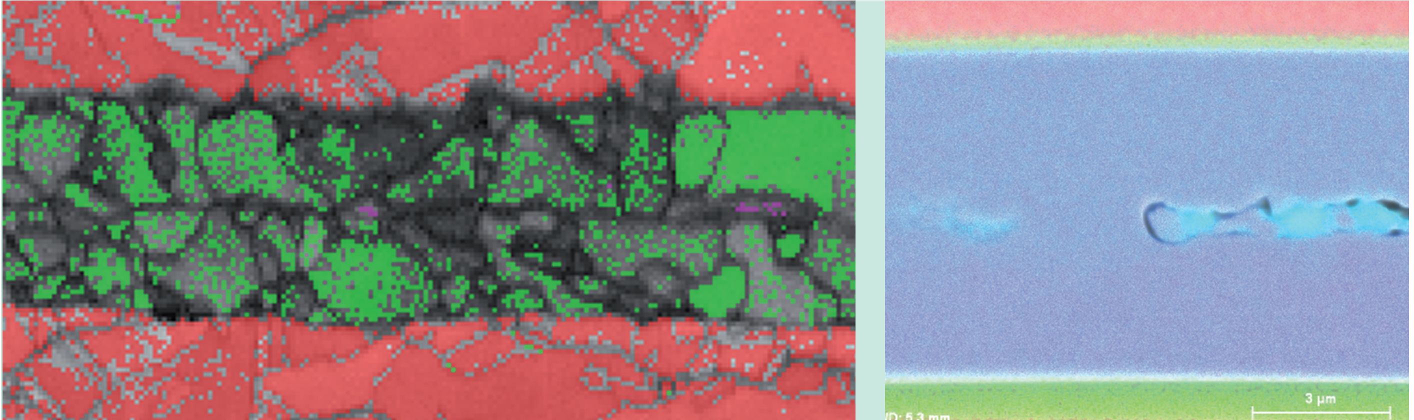
SOLID-LIQUID INTERDIFFUSION BONDING (SLID) AT WAFER LEVEL



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Description

Ongoing miniaturization and steady increase of functionality and complexity of Microsystems and MEMS lead to a strong involvement of 3D integration technologies at chip and wafer level. Existing packaging techniques have to ensure both the mechanical encapsulation of the sensor/actuator and the electrical interconnection to the outer world.
This means that bonding technologies have to be based on conductive materials that enable a hermetic encapsulation. Here metal based intermediate layers are preferred.
SLID bonding is realized by a short liquid phase of one low melting metal and the immediate solidification caused by diffusion and intermixing with a second, high melting metal (Solid-Liquid Interdiffusion – SLID). Ideally a stable intermetallic phase is generated.
Depending on the low melting material some of the combinations allow a process temperature lower than 300 °C. Furthermore there is another advantage: After the stable phase is formed the melting temperature of the alloy is much higher than the bonding temperature and increase the field of applications tremendously.
Today one could find such bonding processes already in chip and component assembly. The goal is to use these principles also for wafer level bonding and 3D integration in MEMS and smart systems development.

Technologies that could be performed

To perform a SLID bonding process the deposition and patterning of certain layers and multi layer systems as well as the right bonding parameters including surface pre treatment steps are important.
Typical layer deposition processes for metal layers are electro chemical deposition (ECD) and physical vapor phase deposition (PVD). Necessary seed layers for ECD were mostly realized with the one of the SLID materials or also with another conductive material. Using a UV-LIGA process a patterned layer deposition of the two materials could be applied (pattern plating). Starting experimental investigations at chip level the evaluation and development could be run to wafer level as well.

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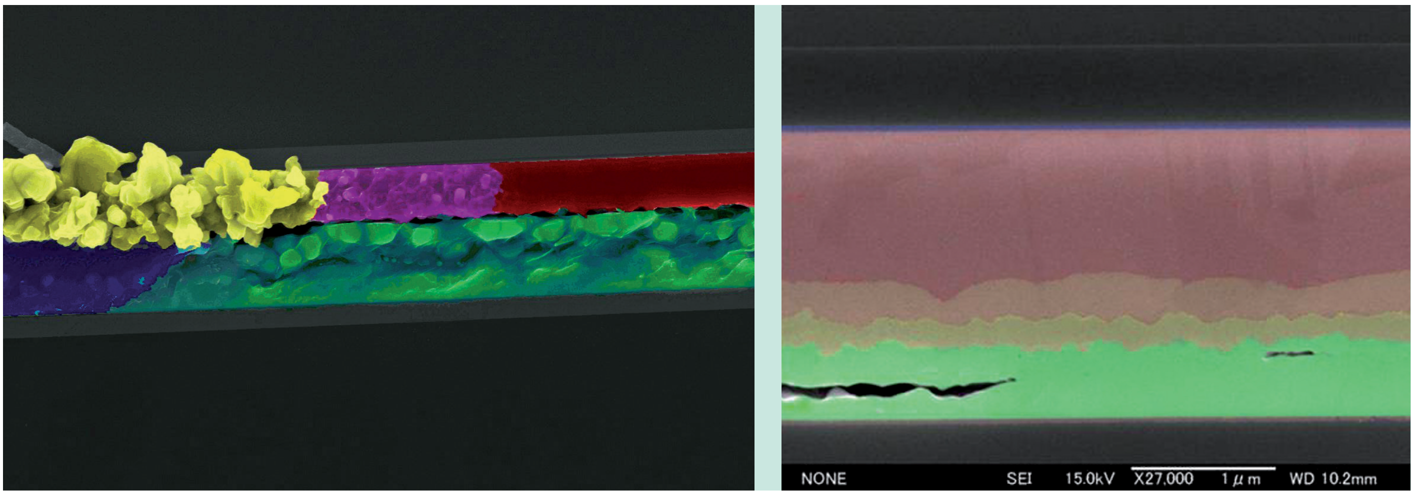

For cleaning and surface pre-treatment certain wet process steps like standard cleaning, etching, CMP are available as well as dry processes like plasma cleaning and gas bubbling (formic acid and forming gas). These processes are necessary for surface cleaning and native oxide removement and to ensure the good contact between the metals of the two wafer surfaces.
After alignment within a usual bond aligner the wafers were processed in a substrate bonder applying temperature, bonding pressure, vacuum and a certain processing time. Fraunhofer ENAS could offer two bonding lines, one from Suss Microtec AG and another from EV Group depending on the customers' interest.
At least the evaluation and characterization of the properties of bonding is done with microstructural analysis using (SAM, IR, REM, EDX, EBSD) but also properties like mechanical strength, hermeticity and electrical conductivity were characterized.

Equipment

- Clean rooms classes ISO 4 – 6
- Mirra and IPEC 472 for CMP (150 mm and 200 mm)
- Lithography
- Deposition by PVD, CVD, ECD (e.g. Cu, Au, Sn, In)
- SUSS Cleaner CL 200
- SUSS bonding aligner BA 6/8
- SUSS substrate bonder SB 6/8e (100 mm to 200 mm)
- EVG aligner 6200NT
- EVG substrate bonder 540HE (100 mm to 200 mm)
- Tira tensile and pressure tester, Micro Chevron test, Blade test
- Tactile and Non-Tactile profilometry
- Light, IR, US, RE and AF microscopy
- White light interferometer
- FTIR spectrometer

Figures:
page 1: left: EBSD analysis shows structures with Cu3Sn phase; right: EDX analysis of an AuSn bond;
page 2: Interface of solid liquid interdiffusion bond based on gallium

Photo acknowledgments: Fraunhofer ENAS
All information contained in this datasheet is preliminary and subject to change. Furthermore, the described systems, materials and processes are not commercial products.